Remarks

Applicant respectfully requests that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicant believes that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1 and 31 have been amended. No claims have been canceled. Therefore, claims 1, 3-31 and 33 are now presented for examination.

Claims 1, 3-10, 31 and 33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Arimilli (U.S. Patent 6,629,268) in view of WO 00/52582 and further in view of Arimilli (U.S. Pub. No. 2002/0129211). Applicant submits that the present claims are patentable over any combination Arimilli 1, Arimilli 2 and WO 00/52582.

Arimilli 1 discloses a method and apparatus for servicing a processing system through a test port allow initialization and fault recovery capability including the ability to coherently access cache memory while the processing system is operating. A JTAG standard interface is used to access registers in a main processing component and has the additional capability to generate internal bus transactions to access registers, cache and memory both within the main processor, and externally by causing a bus interface in the main processor to generate external bus transactions. The service processor can coherently access cache by this mechanism, allowing fault tolerant recovery from operations in which the cache must be coherently flushed in order to maintain proper system operation. See Arimilli 1 at Abstract.

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Arimilli 2 discloses a data processing system and method of operating a data processing system that arbitrate between conflicting requests to modify data cached in a shared state and that protect ownership of the cache line granted during such arbitration until modification of the data is complete. The data processing system includes a plurality of agents coupled to an interconnect that supports pipelined transactions. While data associated with a target address are cached at a first agent among the plurality of agents in a shared state, the first agent issues a transaction on the interconnect. In response to snooping the transaction, a second agent provides a snoop response indicating that the second agent has a pending conflicting request and a coherency decision point provides a snoop response granting the first agent ownership of the data. In response to the snoop responses, the first agent is provided with a combined response representing a collective response to the transaction of all of the agents that grants the first agent ownership of the data. In response to the combined response, the first agent is permitted to modify the data. See Arimilli 2 at Abstract.

WO 00/52582 discloses a cache protocol having a multiple indication such that a part of the MESI state of a memory and the MESI state of an individual processor and/or another cache are indicated. See WO 00/52582 at claim 1.

Independent claims 1 and 31 of the present application each recite a cache line simultaneously having two cache coherency states with a first cache coherency state when accessed from a first interface and a second cache coherency state when accessed from a second interface. Applicant submits that each of the Arimilli 1, Arimilli 2 and WO 00/52582 fail to disclose or suggest *a cache line **simultaneously** having two cache coherency states*. Therefore, any combination of the references would also fail to

disclose *a cache line **simultaneously** having two cache coherency states*. As a result claims 1 and 31, and their respective dependent claims, are patentable over the combination Arimilli 1, Arimilli 2 and WO 00/52582.

Claims 11-30 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Arimilli (2002/0129211) in view of WO 00/52582. Applicant submits that the present claims are patentable over the combination Arimilli 2 and WO 00/52582.

Independent claim 11 of the present application recites transitioning a first cache coherency state to a joint cache coherency state. Applicant submits that nowhere in either Arimilli 2 or WO 00/52582 is there disclosed a process of ***transitioning a first cache coherency state** of a first cache line in a first cache **to a joint cache coherency state***. Particularly, there is no disclosure in either of the references of a ***joint cache coherency state***.

The Examiner maintains that that Figure 3 of the WO 00/52582 reference discloses transitioning a first cache coherency state to a joint cache coherency state. See Final Office Action at page 5, paragraph d. However, applicant respectfully disagrees with the Examiner's construction of the WO 00/52582 reference. Figure 3 of WO 00/52582 shows a state diagram that has expanded states (e.g., SI, ES, MI, MS, etc.), where the first letter of the state title relates to a state in a third level cache (TLC) and the second letter relates to the state in a second level cache (TLC). See WO 00/52582 at Figure 3 and page 12, lines 9-17.

Applicant submits that in no way can an indication combining the status of two separate caches be considered equivalent to a joint cache coherency state of a cache line in a single cache. Because both Arimilli 2 and WO 00/52582 fail to disclose or suggest

transitioning a first cache coherency state of a first cache line in a first cache to a joint cache coherency state, any combination of Arimilli 2 and WO 00/52582 would also fail to disclose or suggest such a feature. Therefore, claim 11 is patentable over the combination Arimilli 2 and WO 00/52582.

Independent claims 14, 18, 21, 24 and 28 include limitations similar to those recited in claim 11. Therefore claims 14, 18, 21, 24 and 28, and their respective dependent claims, are patentable over a combination Arimilli 2 and WO 00/52582 for reasons similar to those recited in claim 11.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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Date: February 28, 2008

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